

### **Amendment to Specification**

Please amend the numbered paragraph below as follows:

**[0061]**        The top surface of polysilicon 170 is not planar in the array area. Layer 170 has protrusions 170.1 over the select gate lines 140. Cavities 170C form in layer 170 between protrusions 170.1 over the future positions of bitline regions 174 (Fig. 30A). The protrusions 170.1 will be used to define the overlap between the floating and control gates without additional dependence on photolithographic alignment.